ANALOG DEVICES

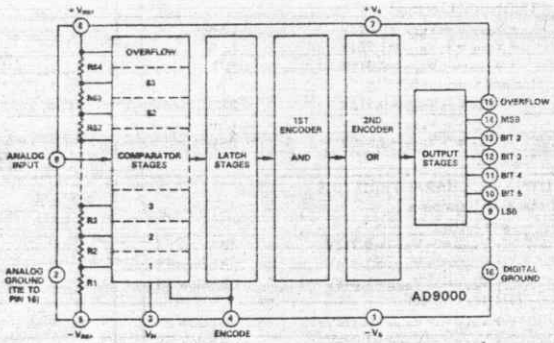
Ultra High-Speed 6-Bit Monolithic ADC

AD9000

FEATURES
- 75MHz Minimum Word Rates
- T/H Required
- −55°C to +125°C Temperature
- Overflow Bit for Cascading Units

APPLICATIONS
- Image Processing
- Video Digitizing
- Radar Digitizing
- Military Systems

AD9000 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

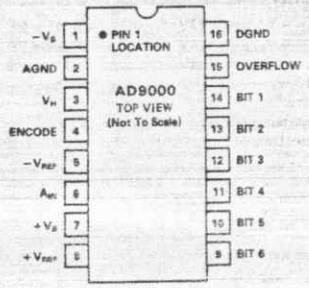
The AD9000 A/D Converter is another addition to the expanding line of monolithic high-speed data converters available from Analog Devices. As model number AD9000SD, this 6-bit, 75MHz A/D can be operated over a temperature range extending from −55°C to +125°C, making it useful for a variety of applications in a wide diversity of environments. For applications requiring operation from 0 to +70°C, the AD9000JD is the recommended device.

The AD9000 is a "flash" converter which uses 64 parallel comparators to digitize fast-moving analog input signals without the need for external track-and-hold (T/H) circuits. An overflow bit can be used for connecting multiple units in a cascade arrangement to obtain up to eight bits of digital data at MHz word rates.

Two cascaded devices can be used to obtain seven bits, and four units will provide eight bits of ECL-compatible output data.

Careful design techniques assure temperature coefficients which allow the unit to be operated over extended temperature ranges. The flexibility and usefulness of the AD9000 are also enhanced by its ability to operate with maximum positive and negative reference voltages applied simultaneously, as contrasted with other flash converters which often limit the user to a small range of voltage within the extremes.

All models of the AD9000 are packaged in standard ceramic DIP 16-pin configurations.



Outline & Pin Designations

10

SPECIFICATIONS (typical @ +25°C and nominal power supplies unless otherwise noted)

Model		AD9000SD			AD9000JD		
Parameter	Units	Min	Typ	Max	Min	Typ	Max
RESOLUTION (FS = Full Scale)	Bits		6			6	
LSB WEIGHT							
$+V_{REF} = -V_{REF} = 0.512V$	mV		16			16	
$+V_{REF} = -V_{REF} = 1.024V$	mV		32			32	
$+V_{REF} = -V_{REF} = 2.048V$	mV		64			64	
DC ACCURACY	%FS ± 1/4LSB		0.4			0.4	
Nonlinearity vs. Temperature	% of FS/°C		0.003			0.003	
Differential Linearity[1]							
$+V_{REF} = -V_{REF} = 0.512V$	LSB		0.75	1.0		0.75	
$+V_{REF} = -V_{REF} = 1.024V$	LSB		0.25	0.5		0.25	
$+V_{REF} = -V_{REF} = 2.048V$	LSB		0.2	0.4		0.2	
Integral Linearity[2]							
$+V_{REF} = -V_{REF} = 0.512V$	LSB		1.25	1.5		1.25	
$+V_{REF} = -V_{REF} = 1.024V$	LSB		0.7	1.0		0.7	
$+V_{REF} = -V_{REF} = 2.048V$	LSB		0.4	0.75		0.4	
Monotonicity		Guaranteed −55°C to +125°C			Guaranteed 0 to +70°C		
DYNAMIC CHARACTERISTICS							
In-Band Harmonics[2]							
(dc to 1MHz)							
$+V_{REF} = -V_{REF} = 0.512V$	dB below FS		44			44	
$+V_{REF} = -V_{REF} = 1.024V$	dB below FS		47			47	
$+V_{REF} = -V_{REF} = 2.048V$	dB below FS		47			47	
(1MHz to 5MHz)							
$+V_{REF} = -V_{REF} = 0.512V$	dB below FS		40			40	
$+V_{REF} = -V_{REF} = 1.024V$	dB below FS		40			40	
$+V_{REF} = -V_{REF} = 2.048V$	dB below FS		41			41	
(5MHz to 8MHz)							
$+V_{REF} = -V_{REF} = 0.512V$	dB below FS		30			30	
$+V_{REF} = -V_{REF} = 1.024V$	dB below FS		30			30	
$+V_{REF} = -V_{REF} = 2.048V$	dB below FS		31			31	
Conversion Time	ns		13			13	
Conversion Rate[3]	MHz	75	100		50		
Aperture Uncertainty (Jitter)	ps		25			25	
Aperture Time (Delay) (T_D)	ns		2			2	
Setup Time (t_s)[4]	ns	2			2		
Hold Time (t_h)[5]	ns	2			2		
Signal Transition Time[6]							
Input to Output Low ($t_{pd}-$)	ns	11	13	14	11	13	14
Input to Output High ($t_{pd}+$)	ns	8	10	12	8	10	12
Signal to Noise Ratio (SNR)[7]							
$+V_{REF} = -V_{REF} = 0.512V$	dB		36			36	
$+V_{REF} = -V_{REF} = 1.024V$	dB		37			37	
$+V_{REF} = -V_{REF} = 2.048V$	dB		36			36	
Signal to Noise Ratio (SNR)[8]							
$+V_{REF} = -V_{REF} = 0.512V$	dB		45			45	
$+V_{REF} = -V_{REF} = 1.024V$	dB		46			46	
$+V_{REF} = -V_{REF} = 2.048V$	dB		45			45	
Noise Power Ratio (NPR)[9]							
$+V_{REF} = -V_{REF} = 0.512V$	dB	27	29			29	
$+V_{REF} = -V_{REF} = 1.024V$	dB	27	29			29	
$+V_{REF} = -V_{REF} = 2.048V$	dB	27	29		27	29	
Transient Response[10]	ns			10			10
Overvoltage Recovery[11]	ns		5			5	
ANALOG INPUT (A_{IN})							
Voltage Range, Rated Performance	V	±0.5		±2			
Input Type		Unipolar (positive or negative) or Bipolar					
Input Current							
Hold (Latch) Mode	μA	−10		+10	−10		+10
Track (Sample) Mode[12]	μA		550	800		550	800
Input Capacitance[13]	pF		30			30	
Impedance[12]	kΩ		3.6			3.6	
Frequency Response[14]							
(75MHz Encode Rate)							
$+V_{REF} = -V_{REF} = 0.512V$	MHz		24			24	
$+V_{REF} = -V_{REF} = 1.024V$	MHz		20			20	
$+V_{REF} = -V_{REF} = 2.048V$	MHz		15			15	
REFERENCE INPUT							
Positive Reference ($+V_{REF}$)	V	−1.5		+2.0	−1.5		+2.0
Negative Reference ($-V_{REF}$)	V	−2.0		+1.5	−2.0		+1.5
Resistance	Ω	80	100	200	80	100	200
Bandwidth							
Small Signal, 3dB	MHz		25			25	
Large Signal, 3dB	MHz		20			20	

Model / Parameter	Units	AD9000SD Min	AD9000SD Typ	AD9000SD Max	AD9000JD Min	AD9000JD Typ	AD9000JD Max
ENCODE COMMAND INPUT							
Logic Compatibility			ECL			ECL	
Digital "1" (Hold/Latch)	V	−1.1	−0.9	−0.6	−1.1	−0.9	−0.6
Digital "0" (Track/Sample)	V	−2.0	−1.7	−1.5	−2.0	−1.7	−1.5
Digital "1" Current	μA	5	15	35	5	15	35
Digital "0" Current	μA	5	15	35	5	15	35
Required Termination (to −2V)	Ω			50			50
Pulse Width							
Hold/Latch [t_{pw}(H)]	ns	5	7		5	7	
Track/Sample [t_{pw}(T)]	ns	4	6		4	6	
Frequency[3]	MHz	75	100		50		
DIGITAL OUTPUT							
Format	Bits		6 Parallel (RZ) plus Overflow (NRZ)				
Logic Compatibility			ECL				
Digital "1"	V	−1.1	−0.9	−0.6	−1.1	−0.9	−0.6
Digital "0"	V	−2.0	−1.7	−1.5	−2.0	−1.7	−1.5
Required Termination (to −2V)	Ω	100			100		
Time Skew	ns			0.4			0.4
Coding			Binary (BIN) Offset Binary (OBN) No Data Ready Output Pulse				
POWER REQUIREMENTS							
+5V ± 5% (+V_S)	mA		60	75		60	75
−5.2V ± 5% (−V_S)	mA		67	85		67	85
Power Dissipation							
(+V_{REF} = −V_{REF} = 0V)	mW		650			650	
(+V_{REF} = −V_{REF} = 1V)	mW		690			690	
(+V_{REF} = −V_{REF} = 2V)	mW		810			810	
TEMPERATURE RANGE							
Operating (Case)	°C	−55		+125	0		+70
Storage	°C	−55		+150	−55		+150
THERMAL RESISTANCE[15]							
Junction to Air, θja (Free Air)	°C/W		95			95	
Junction to Case, θjc	°C/W		20			20	
PACKAGE TYPE[16]			D16A			D16A	

NOTES

[1]Encode Rate = 75MHz; Analog Input = 1kHz.

[2]Spurious in-band signals generated at 20MHz encode rate at analog inputs shown in ( ).

[3]Some spec degradation may occur at word rates (encode frequencies) above minimum shown. See Figure 4 for typical relationship between analog input frequencies and encode rates.

[4]This is internal time set by design and is the minimum time before positive leading edge of Encode Command that a latch output must be at "1" for digital output to be generated by the latch.

[5]This is internal time set by design and is the minimum time after positive leading edge of Encode Comand that a latch output must remain at "1" for digital output to be generated by the latch.

[6]Specifications with digital outputs terminated in 100Ω connected to −2V.

[7]RMS signal to rms noise ratio with 500kHz analog input.

[8]Peak-to-peak signal to rms noise ratio with 500kHz analog input.

[9]DC to 8.2MHz white noise bandwidth with slot frequency of 3.886MHz; and encode rate of 20MHz.

[10]For full-scale step input, 6-bit accuracy attained in specified time.

[11]Recovers to 6-bit accuracy in specified time after 150% FS input overvoltage.

[12]Measured in track (sample) mode with A_{IN} = +V_{REF}.

[13]Measured with A_{IN} = +V_{REF}.

[14]Specified frequencies are maximums with no missing codes.

[15]Recommended maximum junction temperature is +150°C. When using ±2V references, this temperature may be exceeded unless some form of heat sinking and/or cooling air is used. Note θja specification.

[16]See Section 19 for package outline information.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Parameter	Units	Lower Limit	Upper Limit
Supply Voltages			
$+V_S$	Volts	−0.3	+6.0
$-V_S$	Volts	−6.0	+0.3
Analog Input (A_{IN})	Volts	−3.0	+3.0
Encode Command Input	Volts	−6.0	0.0
Reference Inputs			
$+V_{REF}$	Volts	−3.0	+3.0
$-V_{REF}$	Volts	−3.0	+3.0
Hysteresis Control Input	Volts	0	+3.0
Temperature			
Operating			
AD9000SD	°C	−55	+125
AD9000JD	°C	0	+70
Storage	°C	−55	+150
Lead Soldering (10 seconds)	°C		+300

PIN	SYMBOL	FUNCTION
1	$-V_S$	−5.2V NEGATIVE SUPPLY VOLTAGE
2	A_{GND}	ANALOG GROUND
3	V_H	HYSTERESIS CONTROL
4	ENCODE	ENCODE COMMAND INPUT
5	$-V_{REF}$	NEGATIVE VOLTAGE REFERENCE
6	A_{IN}	ANALOG INPUT
7	$+V_S$	+5V POSITIVE SUPPLY VOLTAGE
8	$+V_{REF}$	POSITIVE VOLTAGE REFERENCE
9	BIT 6	LEAST SIGNIFICANT BIT (LSB) OUTPUT
10	BIT 5	BIT 5 OUTPUT
11	BIT 4	BIT 4 OUTPUT
12	BIT 3	BIT 3 OUTPUT
13	BIT 2	BIT 2 OUTPUT
14	BIT 1	MOST SIGNIFICANT BIT (MSB) OUTPUT
15	OVERFLOW	OVERFLOW BIT OUTPUT
16	D_{GND}	DIGITAL GROUND

NOTE: A_{GND} (PIN 2) and D_{GND} (PIN 16) SHOULD BE CONNECTED TOGETHER AS CLOSE TO CASE AS POSSIBLE.

THEORY OF OPERATION

Refer to the Block Diagram of the AD9000.

Reference voltages ($+V_{REF}$ and $-V_{REF}$) applied across an array of identical resistors establish the analog operating span of the unit ($+V_{REF}$) − ($-V_{REF}$). The 64 resistors in the array divide the range into quantization levels equal to intervals of one least significant bit (LSB) between each resistor.

Each tap of the resistor array is connected to its associated voltage comparator input; the other input of each comparator is connected to the analog input (A_{IN}) signal. In this way, the comparator stages simultaneously compare the analog input with each one of the 64 (including OVERFLOW) quantization levels within the analog span set by the reference voltages.

Any comparator whose reference level is less than the analog input voltage will change its output state to a digital "1". Comparators whose reference levels are greater than the analog input will remain at digital "0".

Depending on the value of A_{IN}, anywhere from none to 64 comparators might have digital "1" at their outputs; the remaining comparators will be at digital "0". Obviously, processing that many bits of digital information is impractical if the data remain in this type of unwieldy format.

Wired-or logic circuits within the AD9000 re-encode the comparator outputs into a manageable, binary format of six bits of parallel data; along with an overflow bit which allows cascading units to obtain higher resolution.

The outputs of the comparators are applied to latches controlled by the ENCODE input. When the encode command is low (digital "0"), the latches are transparent; this is the track (sample) mode of the AD9000.

When the ENCODE input changes to high (digital "1"), the latches go into a "hold" (latch) condition, "freezing" the most recent digital outputs of the comparators and applying them to the encoding circuits.

The signal held in the latches is converted to binary form by the encoders and applied to the output stages as a six-bit digital representation of the analog signal which was present at the comparator inputs at the instant the ENCODE command made the change to the "hold" mode.

After 5–7 nanoseconds in the "hold" mode, the ENCODE input again transitions to a "track" condition; and the six bits of parallel data (but not the OVERFLOW output) return to zero (RZ). The "track" portion of the ENCODE command is 4–6 nanoseconds and during this interval the latches respond to the new state of the comparator outputs. The ENCODE signal then transitions again to the hold/latch (digital "1") mode and the cycle repeats. Track mode and hold mode intervals are dependent on duty cycle; times cited here are approximations for an encode frequency of 75MHz.

Time relationships of the hold/latch mode and track/sample mode of the ENCODE command are often influenced by the word rate selected by the user. At higher rates, it may be desirable to shorten the "hold" portion and lengthen the "track" portion; this technique can often enhance overall performance of the unit.

There is no need for an external track-and-hold circuit because the latches are performing the track/hold function. The aperture uncertainty (jitter) and aperture time (delay) specifications shown on the Specifications Table are "worst case" specs for the individual comparator cells, but are valid for the AD9000 because they manifest themselves as converter characteristics.

The good linearity tempco of the AD9000 is the result of using matched diffused resistors in the input network. Linearity in this type of converter is dependent primarily on the tracking of resistors; expressed in another way, resistance ratios are more important than absolute resistance values. Comparator thresholds in the AD9000 remain constant within a small fraction of 1LSB over the complete operating temperature range because of the close tracking of the resistors within the network. The temperature coefficients of comparator input bias currents and initial offset voltages which contribute to nonlinearity are kept small in the design of the AD9000 to minimize their effects.

Low offset voltages in the comparators are critically important for establishing the lower limit of the analog span set by the voltage references. When the reference voltage across the resistor chain decreases (the difference between $+V_{REF}$ and $-V_{REF}$ becomes less), the smaller value of the LSB approaches the value of the "worst case" comparator offset voltage. As the two get closer to one another, increasing linearity errors can restrict the lower limit of the analog span if comparator offset is relatively large.

The upper limit of the analog span is established by the common-mode range of the comparators because this range sets the maximum differential between $+V_{REF}$ and $-V_{REF}$. In this characteristic, too, the design of the AD9000 suggests its use instead of some competing devices.

Unlike some units, the AD9000 allows maximums of positive and negative reference voltages to be applied simultaneously. In some "flash" A/D's, the analog span is limited to some small range within the range of references, as opposed to being equal to the extremes. The ability of the AD9000 to operate with full-scale references improves its usefulness to the designer by imposing fewer constraints on operating conditions.

Like all flash converters, the input resistance of the AD9000 varies as a function of analog input voltage. This is because the individual comparators draw no current until the input voltage exceeds the reference voltage of the comparator; after that, the comparator's input current remains essentially constant. Consequently, the converter's input current and input resistance increase in a series of small steps as successive comparators are operated by an increasing analog input.

The input capacitance of the unit is the sum of the junction capacitances of the individual comparators. For many flash converters, this total is sometime sufficiently high to require a low-impedance driving source for the analog input. In the AD9000, however, input capacitance is typically 30pF, which is considerably lower than many competing devices and imposes fewer restrictions on the driving source.

AD9000 TIMING DIAGRAM

Refer to Figure 1, AD9000 Timing Diagram.

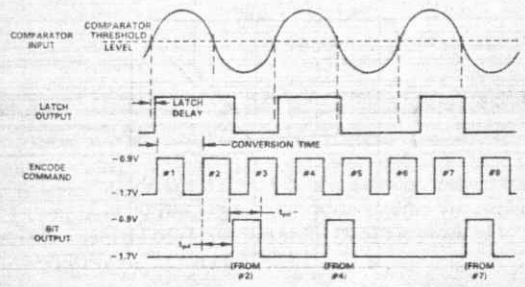


Figure 1. AD9000 Timing Diagram

The comparator input shown on the top of the diagram is the analog input applied to one of the 63 comparators used to establish the digital value of the output word. The latch output is the latch associated with that comparator.

Each time the analog input applied to the comparator exceeds the reference level of the comparator, the corresponding latch output transitions to a digital "1" level.

When the encode command is at $-0.9V$ (digital "1") and the latch outut is at digital "1", a bit output associated with the comparator/latch combination will appear at the output. This statement is true only if:

A. The latch output is at digital "1" for a minimum of two nanoseconds before the positive-going leading edge of the encode signal (t_s).

B. The latch output remains at digital "1" for a minimum of two nanoseconds after the positive-going leading edge of the encode signal (t_h).

In Figure *1*, there is no bit output associated with encode command #1 because the latch output was at the digital "1" level for less than the required two nanoseconds before the encode command changed. Encode command #2 however, combines with the same latch output to cause a bit output to appear.

At first glance, it might appear encode command #5 should combine with the second latch output to cause a bit output. It does not, however, because the latch output did not remain at a digital "1" level for a minimum two nanoseconds after the positive-going leading edge of the encode command.

Like t_s and t_h, the latch delay interval shown in Figure 1 is based on internal timing and is approximately one nanosecond long, but has only academic interest for the user. The important time intervals for proper use of the AD9000 are conversion time (typically 13ns); and signal transition time from the input to a positive output ($t_{pd}+$), and a negative output ($t_{pd}-$). Both signal transition times are typically 10ns.

In Figure 1, the widths of the digital "1" latch signals vary because of interaction with the hold commands. The first one is longer than normal because of encode pulse #2 causing the latch to continue to hold the "1" level. The second latch output is the expected width; while the third is shorter than normal because of encode pulse #6, which delays its transition by keeping it latched at digital "0".

APPLYING THE AD9000

The wired-or logic used in the AD9000 causes the data bits to go low (logic "0") whenever the OVERFLOW bit goes high. This characteristic allows two or more AD9000's to be operated in a cascaded arrangement when more than six bits of resolution are required.

When operating as a single 6-bit A/D, however, that feature of the AD9000 might be undesirable. This is because analog inputs greater than the positive reference voltage will appear as digital outputs of all "0", the same digital output expected of maximum negative inputs. The OVERFLOW bit can serve as a "flag" by going to digital "1" when the positive reference is exceeded.

For some applications, it may be preferable to have the logic output bits "lock up" at digital "1" for positive overvoltages; and digital "0" for negative overvoltages.

This can be accomplished with external logic, as shown in Figure 2, a typical connection for 6-bit operation of the AD9000.

A hex AND gate is used to bring the digital outputs high any time the OVERFLOW bit indicates the positive reference has been exceeded; this gate is wire-ored with the outputs of the AD9000.

Figure 2 contains other details on the preferred method for connecting the AD9000 into circuit applications. The suggested buffer amplifier for the analog input is the Analog Devices'

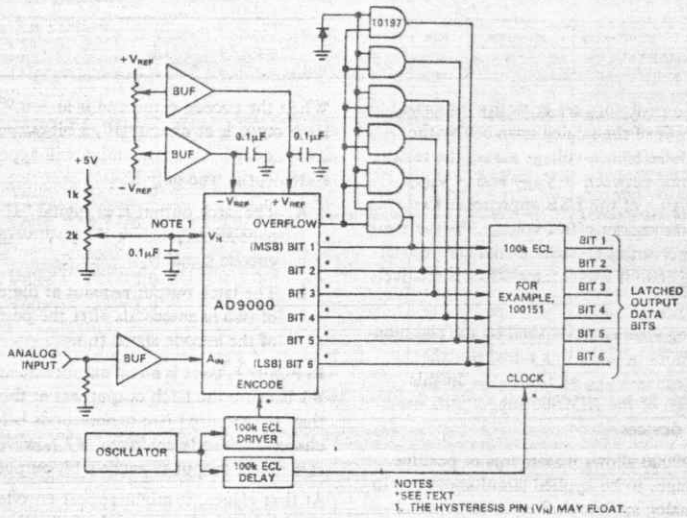


Figure 2. AD9000 6-Bit Operation

ADLH0033 or HOS-100; for the two reference voltages, AD741 devices are recommended. These high performance amplifiers are available in various models, making it easy for the user to select the unit best suited for his application.

The outputs of the reference buffer amplifiers are capacitively bypassed to help prevent noise from interfering with the performance of the AD9000. The ENCODE input is terminated in 50Ω connected to −2V; the CLOCK and digital outputs shown in Figure 2 are terminated in 100Ω, also to −2V.

If preferred, the hysteresis input (V_H) can be left floating, but experience indicates operation of the AD9000 may be improved with a variable voltage applied; this is particularly true at higher word rates.

Refer to Figure 3, which shows the effect of varying hysteresis control voltages.

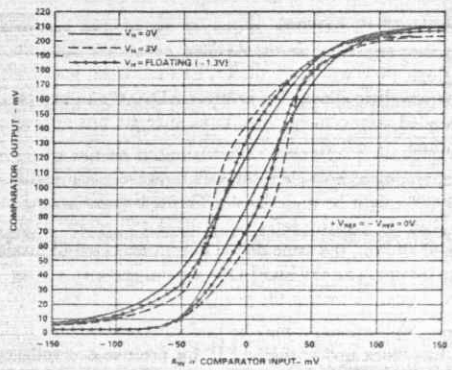


Figure 3. Comparator Output vs. Hysteresis Voltage

In this illustration of a typical comparator's output versus changes in hysteresis voltage, the combination of the two results in a "family" of classic hysteresis curves. The analog input (A_{IN}) voltage is measured in millivolts at the input of the comparator; the other comparator input, of course, is the voltage established by the tap on the resistor array discussed earlier. The comparator output shown on the vertical scale is internal to the AD9000 and appears at the output as an ECL-level signal.

For purposes of discussion of this particular comparator, $+V_{REF} = -V_{REF} = 0V$. Under these circumstances, the threshold of the illustrated comparator is close to 0mV. The thresholds of adjacent comparators would be at slightly different values, but the V_H hysteresis voltage would have the same general effect on the comparators' outputs.

Basically, the variations in hysteresis voltages change the gains of the comparators and slightly alter their outputs, as shown in Figure 3. In many applications, V_H could be left floating, which establishes a hysteresis voltage of approximately +1.3V. In other applications, however, the ability to introduce a small, predictable amount of hysteresis can enhance the AD9000's performance.

The hysteresis control input voltage can vary over a range of 0V to +3.0V, with voltages on the lower end of this span having only negligible effect. Variations between 0V and approximately +0.5V cannot generally be detected as having an impact on the comparator gain.

The interaction between analog input frequencies and the encoding word rate is shown in Figure 4.

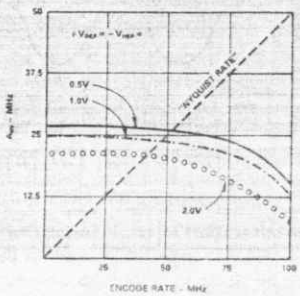


Figure 4. Analog Input vs. Encode Rate

The "Nyquist rate" is shown as a dotted line extending diagonally from dc to an analog input of 50MHz, and a word rate of 100MHz. As illustrated, the range of the analog input reference has a major effect on how closely the AD9000 approaches the Nyquist criteria.

In this figure, the analog input frequencies which are shown are the typical frequencies a user can expect to digitize without

missing codes. Note that as the "spread" of the reference voltages becomes larger, the expected analog input frequency becomes lower.

CASCADING AD9000's FOR MORE BITS

Earlier, there was an allusion to the capability for connecting multiple AD9000 units in a cascade arrangement to obtain more than six bits of digital information. Two cascaded devices would be used to obtain seven bits; and four cascaded devices used for eight bits of output. Although it is theoretically possible to generate multiple bits by employing this method, the practical limitations involved in doubling the number of AD9000's for each additional bit tend to restrict the technique to a maximum of eight bits of digital data.

A possible arrangement for achieving a 7-bit A/D converter is shown in Figure 5.

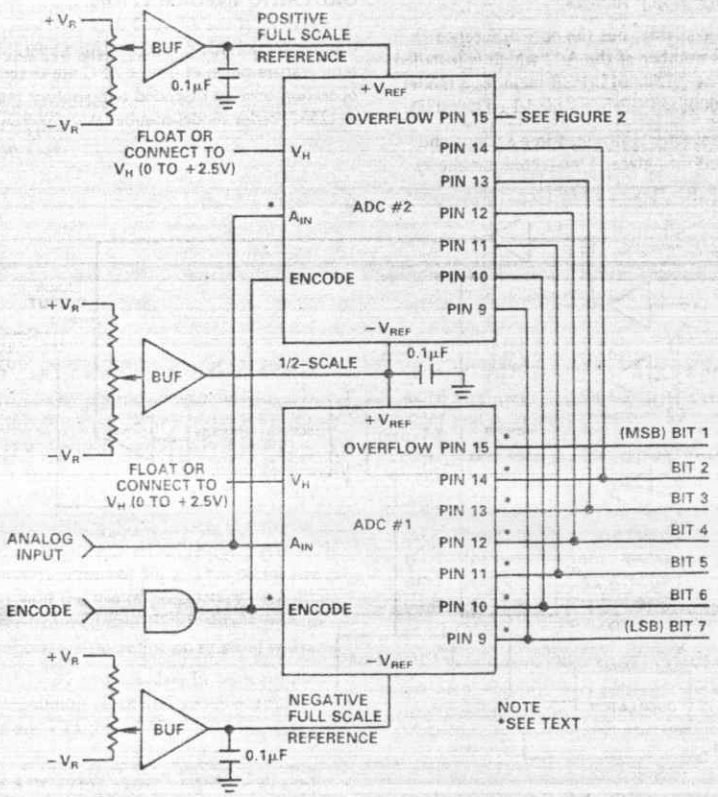


Figure 5. Cascaded AD9000's

When cascading units, the reference-resistor strings are connected in series and driven at the high, low, and mid-scale points. The 6-bit outputs of the two AD9000's are wired together and perform an *or* function; the Most Significant Bit (MSB) is provided by the OVERFLOW output of ADC #1.

If the analog input to the cascaded arrangement is below half-scale, the overflow bit of ADC #2 is low, and so are its output bits. This means the outputs of ADC #1 drive the output lines in response to the analog input.

When the analog input is above half-scale, the OVERFLOW bit of ADC #1 (the MSB) is high and acts as a carry; all the digital output bits of ADC #1 go low. ADC #2 converts the residual upper half-range, and its outputs drive the output lines. The conversions are occurring in parallel, so there is no loss of speed, regardless of whether or not one or both of the cascaded A/D's are operating. The OVERFLOW bit of ADC #2 is wire-ored with external logic in a fashion similar to the method used when operating the AD9000 as a six-bit converter.

If this same technique is expanded to eight bits with four cascaded AD9000 devices, the analog reference span is divided into four equal parts; and a small amount of external logic is used to establish Bit 2 and minimize time skew. The need to double the divisions of the reference span with each succeeding bit is a major deterrent in extending this method beyond eight bits of resolution.

The loads used in cascade are the same as those with a single AD9000, i.e., the ENCODE input is terminated in 50Ω and the CLOCK and digital outputs are terminated in 100Ω, with all loads connected to −2V.

AD9000 EVAULUATION/TEST BOARD

Evaluating and/or testing the AD9000 A/D converter is made easier with the use of a printed circuit board which contains an A/D and the necessary test and reconstruction circuits.

A block diagram of this circuit is shown in Figure 6.

The AD9000 being evaluated or tested is connected in a back-to-back arrangement with a high-speed, high-resolution D/A converter. This combination allows the user to select a reconstructed version of the digitized analog input; or to examine the error signal when checking linearity. All necessary circuit components are contained on the 8.5" × 6.3" printed circuit board; the user needs to provide only power supply voltages.

Two models of boards are available, but the only difference between them is the model number of the A/D which is installed at the time of shipment. The AD9000JD/PCB includes a model AD9000JD unit; the AD9000SD/PCB has a model AD9000SD.

In both boards, the A/D converter is installed in a socket; and all other circuits are soldered into place. This technique allows the evaluation board to be used as a test circuit for incoming AD9000 devices when production quantities are required. Complete operating instructions and a schematic are included with each board.

The test/evaluation board allows the user to check the performance of converters by providing a method for adjusting $+V_{REF}$, $-V_{REF}$, V_H, encode command pulse width, encode rate, and latch strobe delay. This kind of flexibility in assessing the unit's performance can supply valuable insight on how to obtain optimum performance from the AD9000 and get maximum benefit from its characteristics.

ORDERING INFORMATION

All versions of the AD9000 A/D converter are housed in 16-pin ceramic monolithic packages. Units operating over the standard temperature range of 0 to +70°C are designated AD9000JD; for operation over an extended temperature range of −55°C to +125°C, order model number AD9000SD.

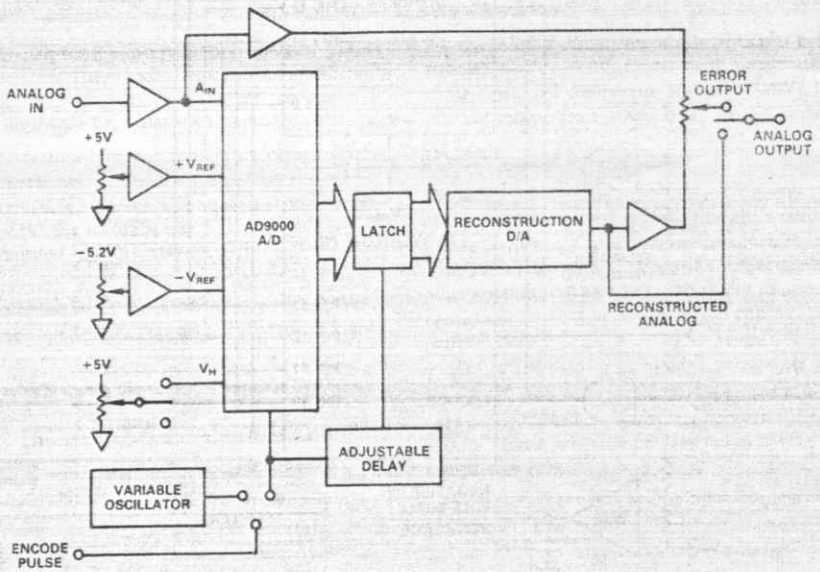


Figure 6. AD9000/PCB Block Diagram